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IN THE UNITED STATES DESIGNATED/ELECTED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY-CHAPTER II

INFORMATION DISCLOSURE STATEMENT
ACCOMPANYING THE FILING OF AN APPLICATION

APPLICANT(S):	Thomas Aeugle et al.
ATTORNEY DOCKET NO.:	P99,1696
INTERNATIONAL APPLICATION NO.:	PCT/EP98/01405
INTERNATIONAL FILING DATE:	11 March 1998
INVENTION:	"METHOD FOR THE PRODUCTION OF A VERTICAL MOS TRANSISTOR"

Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

In accordance with the provisions of 37 C.F.R. § 1.56, Applicant requests that citation and examination of the following references be made during the course of examination of the above-referenced application for United States Letters Patent.

I. SUBMITTED REFERENCES

AA United States Patent No. 5,208,172

AB United States Patent No. 5,545,586

AC United States Patent No. 5,376,562

AL European Application No. 268 941

AM European Application No. 430 514

AN German Application No. 196 21 244

AR R. Loo et al., "Vertical Si p-MOS transistor selectively grown by low pressure chemical vapour deposition", Thin Solid Films, Vol. 294, p. 267 (1997).

AS D. Behammer, "Selectively grown vertical Si-p MOS transistor with short channel lengths", Electronics Letters, Vol. 32, No. 4, p. 406 (15 February 1996).

AT L. Risch et al., "Vertical MOS Transistors with 70nm Channel Length", ESSDERC 1995, p. 101.

AU "Roadmap for Semiconductors", Solid State Technology, Vol. 3, pp. 42 (February 1995).

AV A. Hori et al., "A 0.05µm-CMOS with Ultra Shallow Source/Drain Junctions Fabricated by 5KeV Ion Implantation and Rapid Thermal Annealing", IEDM 94, p. 485.

AW H. Hu et al., "Channel and Source/Drain Engineering in High-Performance Sub-0.1 µm NMOSFETs Using X-Ray Lithography", 1994 Symposium on VLSI Technology Digest of Technical Papers, p. 17.

AX L. Vescan, "Radiative Recombination in SiGe/Si Dots and Wires Selectively Grown by LPCVD", Material Science and Engineering, Vol. 28, p. 173 (1994).

II. EXPLANATION OF RELEVANCE

References AA, AB, AR and AS were cited during earlier PCT examination proceedings. Since references AA, AB, AR and AS are in English, no further commentary concerning their teachings is necessary.

References AC, AL, AM, AN and AT were cited for the reasons noted in a Search Report conducted by the German Patent Office in a counterpart foreign application. A copy of the Search Report is enclosed for the Examiner's review. Reference AL, which is in German, discloses a MOSFET structure with flat source drain zones. Reference AN, which is in German, discloses a semiconductor component, such as a vertical MOS transistor. Since references AC, AM and AT are in English, no further commentary concerning their teachings is necessary.

References AT, AU, AV, AW and AX were cited for the reasons noted in the Applicants' specification. Since references AT, AU, AV, AW and AX are in English, no further commentary concerning their teachings is necessary.

None of the above references discloses or suggests a method for the production of a vertical MOS transistor as disclosed in the present invention.

Copies of each of the above references together with Form 1449 are submitted herewith in accordance with 37 C.F.R. §1.98. The non-English references AL and AN are accompanied by English-language Derwent abstracts. Except as provided, the undersigned does not possess English translations of the non-English references.

This Information Disclosure Statement is being submitted simultaneously with the filing of the present application, and is therefore in compliance with 37 C.F.R. §1.97(b) and no fee is necessary.

All claims of the application are patentable over the teachings of the above references, taken singly or in combination. Early consideration of the application is therefore respectfully requested.

Submitted by,

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37 CFR 1.501
INFORMATION DISCLOSURE STATEMENT
IN A PATENT
(use several sheets if necessary)

Docket No. P99,1696	Serial No.
Applicants **Thomas Aeugle, et al.**	
Filing Date	Group Art Unit

U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If appropriate
	AA	5,208,172	05-04-93	J. Fitch, et al.			
	AB	5,545,586	08-13-96	R. Koh			
	AC	5,376,562	12-27-94	J. Fitch, et al.			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AL	EP 0 268 941	06-01-88	Europe			Abstract	X
	AM	EP 0 430 514	06-05-91	Europe				X
	AN	DE 196 21 244	11-14-96	Germany			Abstract	X
	AO							
	AP							
	AQ							

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	R. Loo, et al., "Vertical Si p-MOS transistor selectively grown by low pressure chemical vapour deposition", Thin Solid Films, Vol. 294, p. 267 (1997)
	AS	D. Behammer, "Selectively grown vertical Si-p MOS transistor with short channel lengths", Electronics Letters, Vol. 32, No. 4, p. 406 (15 February 1996)
	AT	L. Risch, et al., "Vertical MOS Transistors with 70 nm Channel Length", ESSDERC 1995, p. 101
	AU	"Roadmap for Semiconductors", Solid State Technology, Vol. 3, February 1995, pp. 42
	AV	A. Hori, et al., "A 0.05 μm-CMOS with Ultra Shallow Source/Drain Junctions Fabricated by SKeV Ion Implantation and Rapid Thermal Annealing", IEDM 94 p. 485
	AW	H. Hu, et al., "Channel and Source/Drain Engineering in High-Performance Sub-0.1μm NMOSFETs Using X-Ray Lithography", 1994 Symposium on VLSI Technology Digest of Technical Papers, p. 17
	AX	L. Vescan, "Radiative Recombination in SiGe/Si Dots and Wires Selectively Grown by LPCVD", Material Science and Engineering, Vol. 28, p. 173 (1994)

Examiner	Date Considered

***EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**